REMARKS

Claims 1-26 are pending in the present application. Favorable reconsideration and allowance of the application in view of the following remarks are respectfully requested.

Allowable Subject Matter

Applicants note with appreciation that claims 5-9, 12-16, 20-21, and 24 would be allowed if rewritten in independent form including all limitations of the rejected base claims and any intervening claims.

Claim Rejections – 35 U.S.C. § 103 Morikawa in View of Rosner

Claims 1-4, 17-19, 22, 23, and 26 stand rejected under 35 U.S.C. § 103(a) as being obvious over Morikawa et al. (US 2001/0032297 in view of Rosner et al. (US 2004/0221138). Applicant respectfully traverses this art grounds of rejection.

Applicants initially note that the Examiner has maintained his reject reasons outlined in the first Office Action dated June 30, 2006. In addition, in response to Applicants' amendment, the Examiner further alleges that in Morikawa et al. a "target flag" is part of the "first cache memory."

Morikawa et al. teaches that when a processor 1 sends a prefetch instruction. An address buffer 13 compares the content of the two cache tags 11 and 14 to determine whether there is a "hit" or a "miss." If there is a "hit," data is fetched from a naked cache memory 6 or a cache-miss memory 7. If there is a "miss," data from a lower-level memory 9 is stored in the naked cache memory 6 via a data block buffer 18. "[A] target flag 19 that holds storage destination cache information," is set to "0" and "orders the data to be stored in the naked cache memory 6." Paragraphs [0031-0035].

Paragraphs [0035-0038] of the current specification disclose the following.

When a first cache memory 120 receives an interrupt signal INT_ACK, the first cache memory 120 enables a running flag signal RUN_F. The running flag signal RUN_F indicates a state where instructions can be provided to the first cache memory 120. After the first cache memory 120 has output a given number of instructions, the first cache memory 120 disables the running flag signal RUN_F. When the running flag signal RUN_ F is disabled, a second cache memory 130 operates to provide instructions.

As can be seen from the summary of Morikawa et al. and the present application, Morikawa et al. teaches "[A] target flag 19 that holds storage destination cache information," and the present application discloses that the running flag signal RUN_F indicates a state where instructions can be provided to the first cache memory 120. Accordingly, the "target flag 19" of Morikawa et al. is not same thing as the "running flag signal RUN_F," recited in claim 1.

Further, claim 1 recites that the first cache provides instructions when the running flag is enabled, and the second cache provides instructions when the running flag is disabled. Morikawa et al. teaches that if there is a "miss," data from the lower-level memory 9 is stored in the naked cache memory 6 via the data block buffer 18. Accordingly, a combination of the lower-level memory 9 and the target flag 19 is still not the second cache memory recited in claim 1, because the combination of the lower-level memory 9 and the target flag 19 does not provide instructions in response to a disabling of the running flag signal RUN_F to a DSP core. Applicants submit that Morikawa et al. fails to teach or suggest the features recited in claim 1 as alleged by the Examiner. In addition, Rosner et al. fails to cure the deficiency of Morikawa et al.

For at least the reasons given above, Applicants submit that claim 1 is patentable over the combination of Morikawa et al. and Rosner et al.

Independent claim 17 similarly recites the patentable features of claim 1. Therefore, claim 17 is also patentable for all the reasons given with respect to the patentability of claim 1.

Independent claim 22 is a method claim that similarly recites the patentable features of claims 1 and 17. Therefore, claim 22 is also patentable for all the reasons given with respect to the patentability of claims 1 and 17.

Dependent claims 2-4, 18-19, 23 and 26 are also patentable for respectively depending on an allowable base claim.

Claim Rejections – 35 U.S.C. § 103 Morikawa in View of Rosner and Chiu

Claims 10, 11, 13, and 25 stand rejected under 35 U.S.C. § 103(a) as being obvious over Morikawa et al. in view of Rosner et al. and in further view of Chiu et al. (US 2001/0032297). Applicant respectfully traverses this art grounds of rejection.

Without acquiescing to the Examiner allegations, Applicants submit that independent method claim 10 similarly recites the patentable features recited in independent claims 1, 17 and 22 as remarked above. In addition, Chiu fails to cure the deficiencies noted for Morikawa et al. in view of Rosner et al. Therefore, claim 10 is also patentable for all the reasons given with respect to the patentability of claims 1, 17 and 22.

Claims 11, 13 and 25, dependent on claim 10, are patentable at least for the reasons stated above with respect to claim 10.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-26 in connection with the present application is earnestly solicited.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant(s) hereby petition(s) for a one (1) month extension of time for filing a reply to the outstanding Office Action and submit the required $120 extension fee herewith.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By: _____
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